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EXAMINER	
STEVENS, BRIAN J	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/536,719	OCHI, HIROTAKA	
	Examiner	Art Unit	
	Brian J. Stevens	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,8,11,12 and 14* is/are rejected.

7)☒ Claim(s) *4,5,7,9,10 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the first memory, since the claim states a "second memory".

Allowable Subject Matter

3. Claims 4, 5, 7, 9, 10, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1, 3 and 11 are rejected under 35 U.S.C. 102(a) as being anticipated by applicant admitted art of the Publication US 2006/0072379 A1 (See Paragraph [0045]).

Regarding Claim 1, the applicant admitted prior art (See Paragraph [0045]) teaches an adaptive equalization circuit, comprising:

an analog-digital conversion device (See Figure 8, [101]) for sampling signals read from a recording medium (See Paragraph [0050], "which are signals read from the recording medium and sampled by the analog-digital conversion means");

a first digital equalization device (See Figure 8, [102]) for equalizing waveforms of output of said analog-digital conversion device (See Paragraph [0052], "the data by the analog-digital conversion means 101 is equalized by the first digital equalization means 102");

a phase synchronization device (See Figure 8, [103]) for synchronizing phases for signals equalized by said first digital equalization device (See Figure 8, where [103] has an input from the first digital equalization means [102]);

an equalization target value generation device (See Figure 8, [1041]) for generating an equalization target value of said first digital equalization device from the signals having phases being synchronized by said phase synchronization device (See

Figure 8, where the input to [1041] is being fed from [103] which are the signals that were from the first digital equalization device that have the phases being synchronized); and

a first factor computation device (See Figure 8, [802]) for computing tap factors of said first digital equalization device (See Paragraph [0007], "the tap factors of the first digital equalization means 102 are computed by the temporary factor computation means 802") from the output of said analog-digital conversion device (See Figure 8, where the output of the A/D [101] is sent to [802] via a delay and [801]), the signals equalized by said first digital equalization device (See Figure 8, where the output of [102] is sent to [802] via [1031]), and said equalization target value (See Figure 8, where the output of [1041] is sent to [802])

6. Regarding claim 3, the applicant admitted prior art (See Paragraph [0045]) taught the adaptive equalization circuit according to claim 1, as described above. The applicant admitted art further teaches wherein said first digital equalization device is an FIR filter having tap factors of a symmetric type (See Paragraph [0086], "The first digital equalization means 102 is comprised of an FIR filter in the above description, but a new advantage is generated if this filter is constructed to be a tap factor symmetric type", Also See Figure 8, where [102] is considered prior art).

7. Regarding claim 11, the applicant admitted prior art (See Paragraph [0045]) teaches an adaptive equalization method for equalizing signals read from a recording medium to a desired characteristic, comprising:

sampling the read signals (See Figure 8, [101], also see Paragraph [0050], "which are signals read from the recording medium and sampled by the analog-digital conversion means");

equalizing waveforms for the sampled signals (See Figure 8, [102]);

performing phase synchronization for the waveform-equalized signals (See Figure 8, [103], where the equalized waveform signals are being input);

generating an equalization target value (See Figure 8, [1041]) of said waveform equalization from the phase-synchronized signals (See Figure 8, where the output of the phase-synchronized signals [103] are being sent to the target generation [1041]. See Paragraph [0067], "the temporary target value, which is the equalization target value"); and

computing tap factors for said waveform equalization (See Figure 8, [802]) from said sampled signals, said waveform-equalized signals and said equalization target value (See Figure 8, where the sampled signals from [801] are sent as an input, along with the waveform-equalized signals from the output of [103], and the target value from [1041]).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 6 and 12 are rejected under 35 U.S.C. 103(a) as being obvious over applicant admitted art (Figure 8) in view of US 2002/0067677 A1 by Miyashita et al.

10. Regarding claim 2, applicant admitted prior art (See Paragraph [0045]) taught the adaptive equalization circuit according to claim 1, as described above. The applicant admitted art further teaches wherein said equalization target value generation device further comprises a temporary target value generation device for generating a temporary target value (See Figure 8, [1041]. Also See Paragraph [0097], "temporary target values determined by the temporary target value generation means 1041") that is the equalization target value of the phase-synchronized signals (See Paragraph [0067] "For example, in the temporary target value generation means 1041, the temporary target value, which is the equalization target value with the re-sampling frequency"), but does not teach an equalization target phase rotation device for generating a true target value, that is an equalization target value before synchronizing phases by said phase synchronization device, from said temporary target value . Miyashita teaches the knowledge of an equalization target phase rotation device (See Figure 10, [113]) for generating a true target value (See Paragraph [0129]) from a temporary target values (See Figure 10, "Temporary Judgment Output" as the input to [113]), before, or never,

phase synchronization occurs (See Figure 10, where the signal never has phase synchronization performed to it. Also see Paragraph [0112]), is well known in the art.

11. It would have been obvious to one of ordinary skill in the art, having the teachings of the applicant admitted prior art and Miyashita before them at the time the invention was made, to modify the teachings of the applicant admitted prior art to further include teach an equalization target phase rotation device for generating a true target value, that is an equalization target value before synchronizing phases by said phase synchronization device, from said temporary target value. In order to determine the true target value, the process can require indirectly using phase synchronization by using the temporary target value that was determined from the signal after phase synchronization, thus makes the desired result closer to the "true" target value. One of ordinary skill in the art would therefore have been motivated to make the modification of an equalization target phase rotation device for generating a true target value from a temporary target values, before, or never, phase synchronization occurs.

12. Regarding claim 6, the applicant admitted prior art (See Paragraph [0045]) together with Miyashita taught the adaptive equitation circuit according to claim 2, as described above. The applicant admitted further teaches wherein said phase synchronization device is a phase synchronization loop comprising a first interpolation device for interpolating the signals equalized by said first digital equalization device (See Figure 8, [103]. Also See Paragraph [0022], "the phase synchronization means is a phase synchronization loop further comprising first interpolation means for

interpolating signals equalized by the first digital equalization means") and an interpolation position computation device for computing an interpolation position of said first interpolation device from the output of said first interpolation device (See Figure 8, [1032]. Also See Paragraph [0022], "interpolation position computation means for computing an interpolation position of the first interpolation means from the output of the first interpolation means"), the interpolation position of said second interpolation device being computed by said interpolation position computation device (See Figure 8, [1032]. Also See Paragraph [0022], "and the interpolation position of the second interpolation means is computed by the interpolation position computation means". Although it is not taught in figure 8, to have a second interpolation means, it is disclosed that the interpolation position computation means performs a task that is not used), is it not taught said equalization target phase rotation device being a second interpolation device for interpolating said temporary target value and acquiring said true target value. Miyashita taught the said equalization target phase rotation device as described in claim 2 above. Miyashita further teaches where the "said equalization target phase rotation device" (See Figure 10, [113]) is a second interpolation device (See Paragraph [0112], "In the table, the corresponding relationships between the input values and the output values are defined on the basis of the state transition diagram (FIG. 11)") for interpolating said temporary target value (See Figure 10, input to [113] "Temporary judgment output") and acquiring said true target value.(See Paragraph [0113] through [0122]).

13. Regarding claim 12, the applicant admitted prior art (See Paragraph [0045]) teaches an adaptive equalization method for equalizing signals read from a recording medium to a desired characteristic, comprising:

sampling the read signals (See Figure 8, [101]. See Paragraph [0050], "which are signals read from the recording medium and sampled by the analog-digital conversion means");

equalizing waveforms for the sampled signals (See Figure 8, [102] See Paragraph [0052], "the data by the analog-digital conversion means 101 is equalized by the first digital equalization means 102");

performing phase synchronization for the waveform- equalized signals (See Figure 8, [103]);

generating a temporary target value that is an equalization target value of the phase-synchronized signals (See Paragraph [0007], "The signals (analog-digital conversion information) sampled with a frequency that is slightly higher than the read clock frequency of the data by the analog-digital conversion means 101 is equalized by the first digital equalization means 102");

computing tap factors for said waveform equalization (See Figure 8, [802]) from said sampled signals, said waveform-equalized signals and said equalization target value (See Figure 8, where the sampled signals from [801] are sent as an input, along with the waveform-equalized signals from the output of [103], and the target value from [1041]); but does not teach

generating a true target value, that is an equalization target value before performing phase synchronization, from said temporary target value. Miyashita teaches the knowledge of generating an equalization target value (See Figure 10, [113]) from a temporary target values (See Figure 10, "Temporary Judgment Output" as the input to [113]), before, or never, phase synchronization occurs (See Figure 10, where the signal never has phase synchronization performed to it. Also see Paragraph [0112]), is well known in the art.

14. It would have been obvious to one of ordinary skill in the art, having the teachings of the applicant admitted prior art and Miyashita before them at the time the invention was made, to modify the teachings of the applicant admitted prior art to further include to generate a true target value, that is an equalization target value before performing phase synchronization, from said temporary target value. In order to determine the true target value, the process can require indirectly using phase synchronization by using the temporary target value that was determined from the signal after phase synchronization, thus makes the desired result closer to the "true" target value. One of ordinary skill in the art would therefore have been motivated to make the modification so to generate an equalization target value from a temporary target values, before, or never, phase synchronization occurs.

15. Claim 8 is rejected under 35 U.S.C. 103(a) as being obvious over applicant admitted art (Figure 8) in view of US 6,246,864 B1 by Koike

16. Regarding claim 8, the applicant admitted prior art (See Paragraph [0045]) taught an adaptive equalization circuit according to claim 3, as described above. The applicant admitted prior art further teaches wherein said first factor computation device (See Figure 8, [802]) supplies the computed tap factors to the first digital equalization device (See Figure 8, where the output of [802] is supplied to the first digital equalization device [102] via [803]) and performs adaptive equalization (See Abstract, "and the tap factors of the pre-digital equalization means (102) can be adaptively computed"), but does not teach even if phase synchronization performed by said phase synchronization device is in an unlock status. Koike teaches the knowledge of performing another task although the phase synchronization device is in an unlock status (See Column 2, Line 64 through Column 3, Line 3), is well known in the art.

17. It would have been obvious to one of ordinary skill in the art, having the teachings of the applicant admitted prior art and Koike before them at the time the invention was made, to modify the teachings of the applicant admitted prior art to further include to perform computation even if phase synchronization performed by said phase synchronization device is in an unlock status. In order to obtain a result that has no connection to the idea of having phase synchronization, the obvious modification would be fore the process to continue although phase synchronization has not occurred. One of ordinary skill in the art would therefore have been motivated to make the modification to perform another task although the phase synchronization device is in an unlock status.

18. Claim 14 is rejected under 35 U.S.C. 103(a) as being obvious over applicant admitted art (Figure 8) in view of US 2003/0156603 A1 by Rakib et al.

19. Regarding claim 14, the applicant admitted prior art (See Paragraph [0045]) teaches an adaptive equalization circuit, comprising:

an analog-digital conversion device (See Figure 8, [101]) for sampling signals read from a recording medium (See Paragraph [0050], "which are signals read from the recording medium and sampled by the analog-digital conversion means");

a first digital equalization device (See Figure 8, [102]) for equalizing waveforms of output of said analog-digital conversion device (See Paragraph [0052], "the data by the analog-digital conversion means 101 is equalized by the first digital equalization means 102");

a phase synchronization device (See Figure 8, [103]) for synchronizing phases for signals equalized by said first digital equalization device;

a frequency information threshold device (See Figure 4, [402], where Figure 4 is depicting [1032] of Figure 8, which is prior art) for judging frequency information of said phase synchronization device in a plurality of statuses using one or more threshold values (See Paragraph [0073]);

a status change factor supply device (See Figure 8, [802]) for supplying a tap factor (See Paragraph [0007], "the tap factors of the first digital equalization means 102 are computed by the temporary factor computation means 802 ") corresponding to said status to said first digital equalization device when the status judged by said frequency information threshold device changes (See Figure 8, where the inputs to [802] are from

the first digital equalization device [102] and from frequency information threshold device [1032], that contains [402]), but does not teach

a second memory for previously storing tap factors corresponding to the plurality of statuses judged by said frequency information threshold device respectively. Rakib teaches the knowledge of having a memory to store tap factors based upon a plurality statuses that are judged via a threshold (See Paragraph [0592], "If it is not less than this threshold, the rotational amplifier has falsely locked, and processing proceeds to step 1538 to correct the situation by loading the SE main tap correction factor into the memory", where there are two different statuses based upon a threshold, and depending on that status storing tap factors), is well known in the art.

20. It would have been obvious to one of ordinary skill in the art, having the teachings of the applicant admitted prior art and Rakib before them at the time the invention was made, to modify the teachings of the applicant admitted prior art to further include a second memory for previously storing tap factors corresponding to the plurality of statuses judged by said frequency information threshold device respectively. Once the tap factors have been determined from the frequency information threshold device, the tap factors would be stored, thus making it useful by other devices within the circuit to use at a later time. One of ordinary skill in the art would therefore have been motivated to make the modification so to include a memory to store tap factors based upon a plurality statuses that are judged via a threshold.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian J. Stevens whose telephone number is (571)270-3623. The examiner can normally be reached on M-F 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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